



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

CG

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|----------------------------------------------------------------------------------|-------------|-------------------------|---------------------|------------------|
| 10/079,811 | 02/22/2002 | Andrew Mark Nightingale | 550-318 | 5550 |
| 23117 | 7590 | 03/21/2006 | EXAMINER | |
| NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203 | | | PATEL, SHAMBHAVI K | |
| | | ART UNIT | | PAPER NUMBER |
| | | 2128 | | |

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/079,811 | NIGHTINGALE ET AL. |
| | Examiner | Art Unit |
| | Shambhavi Patel | 2128 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 December 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-16 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 21 December 2005 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

| | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-16 are pending.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 0109282.4 filed on 04/12/01.

Information Disclosure Statement

The information disclosure statement filed on 2/22/02 complies with the provisions of MPEP § 609. It has been placed in the application file. The information referred to therein has been considered as to the merits. (see attached PTO-1449 form).

Response to Arguments

Applicant's arguments filed 12/21/05 have been fully considered but they are not persuasive.

The Applicant has presented the following arguments:

- a. Regarding **claims 1, 15, and 16**, Hollander (US Patent No 6,182,258) fails to disclose the method step of "generating" during modeling of

the software and hardware components and the interaction between the hardware and software components, both a software stimulus for the software component and a hardware stimulus for the hardware component.

- b. Regarding **claims 1, 15, and 16**, Hollander fails to disclose that the modeled interaction between the software component and the hardware component proceeds independently of the hardware and the software stimulus.
- c. Regarding **claims 1, 15, and 16**, Platt fails to disclose using a remote procedure call to pass data between two software processes.
- d. Regarding **claims 3-5**, the combination of Hollander/Platt/Campbell fails to disclose the subject matter of Applicants' independent claims.
- e. Regarding **claim 13**, there is no allegation that the step is disclosed in any of the three cited references.

Regarding the first argument, the Examiner asserts that Hollander discloses generating both a software stimulus for the software component and a hardware stimulus for the hardware component (column 6 lines 50-55; column 10 lines 59-64). There is a co-verification extension module that is built on top of the apparatus. Thus, the software verification is treated as part of the verification effort. Test generation, and result checking combines information from both the hardware and software components (column 10 lines 51-56).

Regarding the second argument, the Examiner asserts that Hollander discloses that the modeled interaction between the software component and the hardware component proceeds independently of the hardware and software stimulus (column 5 lines 21-24; column 8 lines 24-32). As can be seen in figure 1 of the Hollander reference, there is a separate module for generating the stimuli (generate 26) and checking the results (checker 30). When using both dynamic testing and dynamic checking, the test generator module and the checker can synchronize with one another.

Regarding the third argument, the Examiner asserts that Platt teaches using a remote procedure call in order to execute a designated program (Platt column 10 lines 16-22). The applicant is directed to using a remote procedure call as a communication means between the test controller and the simulator, both of which are software modules. Similarly, Platt teaches using the remote procedure call as communication means between two separate software processes.

Regarding the fourth argument, the Examiner asserts that Campbell teaches the steps claimed in claims 3-5. The claims are directed towards determining when the stimulus is ready for the simulation program. When it is ready, a start flag is set high. Similarly, Campbell teaches a method wherein a start flag is used to indicate to a different program that a condition has been met (figure 18).

Regarding the fifth argument, the Examiner asserts that Harmon teaches a co-verification environment that uses an instruction set simulator (column 4 lines 12-16). The ISS is used to simulate an instruction stream in software (column 6 lines 26-34).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 6, 7-12, 14, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (US Patent No 6,182,258) in view of Platt et al (US Patent No. 5,835,764), herein “Platt”.

As per claims 1, 15, and 16, Hollander is directed to a method of simulating a system having a software component (Hollander Column 10 Lines 24-28) and a hardware component (Hollander Column 10 Lines 24-28), said method comprising the steps of:

- a. *Modeling operation of said software component using a software simulator* (Hollander Column 8 Lines 39-44, Column 10 Lines 51-58);
- b. *Modeling operation of said hardware component using a hardware simulator* (Hollander Column 8 Lines 39-44, Column 10 Lines 51-58);
wherein
- c. Said hardware simulator and said software simulator are *linked to model interaction* between said hardware component and said software component (Hollander Column 10 Lines 34-49);
- d. Generating with a test controller (Hollander Figure 1 controller 26, Column 4 Lines 66-67, Column 5 Line 1) a *software stimulus* (Hollander Column 10 Lines 59-61) for said software component and a *hardware stimulus* (Hollander Column 2 Lines 25-27, Column 7 Lines 12-14) for said hardware component so as to permit *verification of correct interoperability* of said software component and hardware component (column 10 lines 51-57), wherein said modeled interaction between said components proceeds *independently of test controller* (figure 1; column 5 lines 21-24; column 8 lines 24-32).

Hollander fails to disclose a method where said software stimulus (Hollander Column 10 Lines 59-61) is passed to said software simulator (Figure 4 simulator 36) by

issuing a remote procedure call from said test controller (Hollander Figure 1 controller 26, Column 4 Lines 66-67, Column 5 Line 1) to said software simulator.

However Platt teaches an analogous method where a system call is made to execute a designated program, using the arguments supplied. When a program needs to be executed, the currently executing process makes a system call requesting that the program be executed. The scheduler makes an entry into the entry table and extracts the information needed to execute the program (Platt Column 10 Lines 16-22).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Hollander and Platt.

The motivation for doing so would have been to develop a method of communication that exhibits high performance (Platt Column 7 Lines 32-36). While other communication protocols are cumbersome and time-consuming (Platt column 5 lines 12-15), the method disclosed by Platt would overcome those deficiencies.

As per **claim 2**, Platt teaches the use of a shared memory to store and retrieve information needed to execute the program. The user writes the information needed for the program execution to the main memory, and the scheduler extracts the information when it receives the request to execute the program (Platt column 7 lines 1-26). The information needed to execute the program is analogous to the software stimuli in claim 2. The user is analogous to said test controller. The scheduler is analogous to said software simulator. The information extracted by the scheduler is analogous to the software stimuli.

As per **claim 6**, Platt teaches that when a request is made for a program to be executed, the request is in the form of a process. The process consists of the executable program and all the information needed to run the program. The receiver of the request can then send back the appropriate response. (Platt column 9 lines 34-36, column 10 lines 16-22).

As per **claim 7**, Hollander is directed to the method as claimed in claim 1 wherein said hardware component is a hardware peripheral within a data processing system (Hollander column 11 lines 29-38).

As per **claim 8**, Hollander is directed to a method as claimed in claim 1 wherein said software component is a software driver for said hardware component (Hollander column 11 lines 29-38, column 3 lines 10-13, column 6 lines 22-24).

As per **claim 9**, Hollander is directed to a method as claimed in claim 1, further comprising monitoring modeled signals at an interface with said hardware component that are generated in response to simulation of said software component and said hardware component (Hollander column 4 lines 52-56, column 8 lines 13-17).

As per **claim 10**, Hollander is directed to a method as claimed in claim 9, wherein said modeled signals are monitored for compliance with rules defining permitted values for said modeled signals (Hollander column 8 lines 13-17).

As per **claim 11**, Hollander is directed to a method as claimed in claim 1, wherein said software simulator is monitored to determine coverage of a range of software stimuli that may be applied to said software simulator (Hollander column 5 lines 32-33, column 8 lines 44-67, column 10 lines 51-55).

As per **claim 12**, Hollander is directed to a method as claimed in claim 1, wherein said hardware simulator is monitored to determine coverage of a range of hardware stimuli that may be applied to said hardware simulator (Hollander column 5 lines 32-33, column 8 lines 44-67, column 10 lines 51-55).

As per **claim 14**, Hollander is directed to a method as claimed in claim 1, further comprising monitoring said hardware simulator to detect expected changes of state within said hardware component occurring in response to said software stimulus (Hollander column 10 lines 51-68).

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (US Patent No 6,182,258) and Platt et al (US Patent No. 5,835,764), herein “Platt” as applied to claims 1-2 above and in further view of Campbell (US Patent No. 6,408,009).

As per **claim 3**, Hollander fails to disclose a method as claimed in claim 2 wherein said test controller sets a start flag within shared memory to indicate to said

software simulator that said shared memory contains call data specifying a software stimulus be modeled.

Campbell teaches a method where a start flag in the program is used to inform the program later on that a condition has been met. In Figure 18, steps 1000, 1002, 1004, and 1020 form that main part of the loop that relies on the start flag. The process starts at step 1000. In step 1002, the start flag is tested to determine whether or not it has been set high. If the start flag has not been set high, it loops back around to step 1002. If it has been set high, the rest of the program may execute, beginning with step 1004, and ultimately ending at step 1020 where the start flag is set low again to indicate that the program is finished executing.

It would have been obvious to combine the teachings of Hollander, Platt, and Campbell. Though Hollander and Platt describe a system to co-simulate a hardware and software component using appropriate communication protocols, both fail to teach what will trigger and control the flow of the program.

The motivation for doing so would be to incorporate an effective method for determining that the stimulus has been received and therefore the simulation can begin.

As per **claim 4**, a method as claimed in claim 3 wherein said software simulator polls said start flag to determine if there is a software stimulus to be modeled is contained in the above combination method of Hollander, Platt, and Campbell. (Campbell Figure 18 steps 1000, 1002)

As per **claim 5**, a method as claimed in claim 3, wherein said software simulator resets said start flag to indicate to test controller that modeling of said software stimulus has been completed is contained in the above combination method of Hollander, Platt, and Campbell (Campbell Figure 18 steps 1020).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (US Patent No 6,182,258) in view of Platt et al (US Patent No. 5,835,764), herein “Platt” as applied to claim 1 above in further view of Harmon (US Patent No. 6,810,373).

Hollander fails to disclose a method as claimed in claim 1, wherein said software simulator is an instruction set simulator that serves to model execution of software program instruction by a data processing core.

Harmon teaches an analogous method wherein the co-verification environment contains an instruction set simulator (ISS) for representing the operation of the processor (Harmon column 3 lines 6-15). Therefore, the hardware is modeled by the logic simulator while the software is simultaneously modeled by the ISS.

At the time of the invention it would have been obvious to combine the teachings of Harmon with the above combination of Hollander and Platt.

The motivation for doing so would have been to increase the performance of the system. By using an ISS, the speed of verification is greatly increased. (Platt column 2 lines 66-67, column 3 lines 1-2, 46-57).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is 571 272 5877. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kamini Shah
KAMINI SHAH
SUPERVISORY PATENT EXAMINER